

**REMARKS**

By the above actions, claims 28-41, 45, 47 and 48 have been amended, new claims 55-63 have been added and claims 42 and 43 cancelled. Claims 28-41, 45, 47, 48 and 55-63 are currently pending. In view of these actions and the following remarks, further consideration of this application is now requested.

The Examiner's allowance of claims 28, 29 and 34-36 and the indication that claims 42 and 43 would be allowable if properly amended is greatly appreciated. Further, it is noted that claims 30-33, 37-40, 47 and 48 were not rejected over prior art. Therefore, it is assumed that claims 30-33, 37-40, 47 and 48, if properly amended to overcome the formality rejection, under 35 U.S.C. § 112 (second paragraph) would also be allowable.

With regard to the Examiner's formality rejection, under § 112 (second paragraph), of claims 30-33, 37-40, 47 and 48, the attached amendments to the claims are believed sufficient to overcome each of the deficiencies noted by the Examiner. Specifically, claims 30 and 37 have been amended to clearly define the second wiring layer as having two portions, i.e., a first portion composed of a laminate of a first and third conductive layers and a second portion composed of a laminate of first, second and third conductive layers. Further, claims 33, 40, 47 and 48 have been amended to clarify alleged indefinite terminology and dependency. For these reasons, the rejection, under § 112 (second paragraph), of claims 30-33, 37-40, 47 and 48 is believed to no longer be appropriate and should now be withdrawn.

Turning to the prior art rejection of claims 41 and 45, under 35 U.S.C. 103(a), as being obvious in view of the teachings of Lee et al. ('150) combined with the teachings of Vu et al. ('963), the Applicants respectfully traverse this rejection. Specifically, the Applicants note that Vu et al. recite (see column 2, lines 10-15) that fabricating an entire matrix display as a single unit leads to unacceptable product yields and quality problems; therefore, Vu et al do not intend or disclose forming the entire active matrix display, i.e., pixel matrix circuit and driver circuit, on a single substrate. For this reason

alone, one of ordinary skill in the prior art would not be taught to combine the teachings of Vu et al with those of Lee et al., who does form the entire active matrix display, i.e., pixel matrix circuit and driver circuit, on a single substrate.

Additionally, the presently claimed invention requires that the n-channel TFTs having the same structure are formed on the same substrate and have either the GOLD structure (gate voltage applied to the LDD region) or the LDD structure, as discussed at paragraphs [0008] and [0054] of the specification. By keeping the first wiring line of the pixel TFT at a fixed electric potential or a floating electric potential, an LDD structure can be achieved. With the LDD structure, holes generated by hot carrier injection can be removed from the channel formation region, and then the electric charge is neutralized to cause the hot carrier to disappear. This results in an increase in the OFF current being contained effectively, as discussed in paragraphs [0051] and [0052] of the specification.

Further, by keeping the claimed first wiring line of the n-channel TFT, included in the driver circuit, at the same level of electric potential as the second wiring line of the n-channel TFT, also included in the driver circuit, the GOLD structure results. This means degradation of the ON current is prevented, as discussed at paragraphs [0031] and [0162] of the specification. That is, the presently claimed invention of claim 41 achieves a CMOS circuit with a very high reliability without the necessity of increasing the number of manufacturing steps, as discussed in the specification at paragraph [0054] and [0162].

Contrary to the Examiner's assertion, neither Lee et al. or Vu et al. teach or even remotely suggest this feature which, as discussed above, is not merely a method of operating limitation but instead provides a definitive structure to the claimed device. Further, the Examiner has provided no well reasoned technical explanation or documentation to support the assertion that the device, resulting from the combined teachings of Lee et al. and Vu et al, has features of the claims described above.

Therefore, since each feature of the claimed invention is not taught or suggested by the proposed combination of teachings of Lee et al. and Vu et al and since there is no motivation or suggestion to combine the teachings of Lee et al with those of Vu et al.

(given the negative teachings of Vu et al regarding formation of a pixel matrix circuit and driver circuit on a single substrate), it is respectfully requested that the rejection of claims 41 and 45, under §103(a), be withdrawn.

New claims 55-63 are added to recite features of the present invention to which Applicants are entitled. Specifically, claims 55 and 58 recite the features of canceled claims 42 and 43 which were designated as containing allowable subject matter. Claims 56-57 and 59-63 depend from claims 55 and 58, respectively, and, thus, should likewise be considered allowable.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with applicant's representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Lastly, it is noted that a separate Extension of Time Petition (one month) accompanies this response along with a check in payment of the requisite extension of time fee. However, should that petition become separated from this Amendment, then this Amendment should be construed as containing such a petition. Likewise, any overage or shortage in the required payment should be applied to Deposit Account No. 19-2380 (740756-2296).

Respectfully submitted,



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